Claims:

1. A data storage device comprising:

a plurality of arrays of physical memory storage elements each having a corresponding respective physical address each said memory storage element capable of storing at least one bit of data; and

address conversion means for converting between a plurality of logical addresses and a said plurality of physical addresses;

wherein said address conversion means comprises at least one memory area storing address translation data describing a plurality of ranges of logical addresses, and for each said range of logical addresses a corresponding respective range of said physical addresses.

2. The data storage device as claimed in claim 1, wherein said address translation data comprises:

a plurality of data entries, each describing the first physical address of a plurality of contiguously addressed physical memory elements, said physical address data being specified in terms of a block address data describing a block of physical addresses, and each describing at least one logical address corresponding to said physical address;

a row address data describing a row of individual memory components, each said memory component comprising an array of a plurality of said memory elements; and

a segment address data, said segment address data specifying a segment of each of a plurality of segments of a plurality of said components,

wherein a relationship between adjacent data entries defines ranges of said logical addresses.

3. The data storage device as claimed in claim 1, wherein said address translation data is stored at least once within said memory storage elements of said data storage device.

4. The data storage device as claimed in claim 1, wherein said plurality of arrays of memory storage elements comprise a plurality of individual memory storage components, each comprising a corresponding respective said array of memory elements, the plurality of memory components arranged in a component array on one or more circuit boards, and connected together by a common physical address bus.

5. The data storage device as claimed in claim 1, comprising a plurality of data entries each defining a relationship between a said logical address and a said physical address, wherein each said row is indexed by a separate index number.

6. The data storage device as claimed in claim 1, wherein said memory storage elements comprise magnetic random access memory elements.

7. A method of converting between a logical address of a data storage device, and a physical address corresponding to individual memory elements within said data storage device, said method comprising the steps of;

(i) storing in a data translation table, address data describing a plurality of logical addresses and a plurality of said physical addresses, wherein each said logical address corresponds to a respective physical address and is assigned an index value;

(ii) reading logical address request data describing a logical address of data to be retrieved;

(iii) reading said stored address data and comparing said read logical address with a said stored logical address data at a first said index value;

(iv) if said logical address of said data to be retrieved is greater than or equal to a look up logical address corresponding to said index of said data entry, incrementing said index value;

(v) repeating steps (i) to (iv) above; and

(vi) determining a physical address corresponding to said logical address to be retrieved as being the sum of the physical address of the previous data entry and the difference between the logical address to be retrieved and the logical address of the previous data entry.

8. A method of interfacing a data storage device comprising an array of a plurality of memory elements, with a logical address bus on which a plurality of logical address data is carried for identifying data stored in said memory device, said method comprising the steps of:

storing a data translation table comprising a plurality of data entries, each said data entry comprising a look up logical address value being a logical address stored in said data translation table and a look up physical address value, said look up physical address value corresponding to a physical location of one or more said memory elements;

upon receipt of a requested logical address, parsing said data entries in said data table, to read a look up logical address of each of a plurality of said data entries;

comparing said look up logical address with said requested logical address;

if a said look up logical address is less than said requested logical address, continuing to parse said data translation table;

if a said look up logical address is less than or equal to said requested logical address, determining a corresponding respective physical address to said requested logical address as being said requested logical address, minus a look up logical address of a preceding data entry in said data translation table, plus a look up physical address corresponding to said preceding data entry in said data translation table.

9. A method of interfacing a data storage device comprising an array of a plurality of memory elements, with a logical address bus on which a plurality of logical address data is carried for identifying data stored in said memory device, said method comprising the steps of:

storing a data translation table comprising a plurality of data entries, each said data entry comprising an indexation number, a logical address value and a physical address value, said physical address value corresponding to a physical location of one or more said memory elements;

detecting at least one defective memory element;

locating a pair of entries within said data translation table which define a range of physical addresses encompassing the address of the defective memory element;

inserting two additional entries in said data translation table between said pair of entries;

creating a first additional data entry in said data translation table, said first additional data entry comprising a logical address which corresponds to the first defective element of the group of defective elements and a physical address being that of a group of previously unused (spare) storage elements;

creating a second additional data entry in said data translation table, said second data entry comprising the logical address corresponding to the physical address subsequent to the highest addressed element of the group of defective elements and that same physical address as the physical address.